Exam 2- key

Question 1:

(5 Pts.) DRAM – Slower; Refresh needed; 1T Cell

(5 Pts.) SRAM – Faster; Does not need refresh; 6T Cell

Question 2:

* (4 Pts.) Memory banks independently accessed, data sequentially stored across banks
* (3 Pts.) Spatial locality
* (3 Pts.) Improves throughput

Question 3:

* (5 Pts.) Seek time: Time to move head to requested track
* (5 Pts.) Rotational delay: Time to move the beginning of the sector to reach the head

Question 4:

* (5 Pts.) Access time = Seek time + Rotational time
* (5 Pts.) Transfer time=Time to transfer data following access time

Question 5: (Any two – each 5 Pts.)

Error correction techniques:

* Parity
* Hamming code
* Mirroring / Redundancy

Question 6: (Any two – each 5 Pts.)

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| --- | --- | --- | --- | --- |
|  | **Density** | **Cost** | **Write** | **Application** |
| NAND | High | Low | Block Erase & Write | Secondary storage |
| NOR | Low | High | Bit | BIOS |

Question 7:

|  |  |  |
| --- | --- | --- |
|  | **Memory Mapped I/O** | **Isolated I/O** |
| (4 Pts.) | Single address space | Separate address space |
| (3 Pts.) | Use same instructions as memory; Richer instruction set | Special instructions; e.g., In and Out |
| (3 Pts.) | No additional lines | M/I/O Line |

Question 8: (2.5 pts. For each cell item)

|  |  |  |
| --- | --- | --- |
|  | **Programmed I/O** | **Interrupt driven I/O** |
| **Overhead** | Busy wait | Context switch |
| **Application** | e.g., Critical devices; Dedicated devices | e.g., Device drivers |

Question 9:

* (10 Pts.) When DMA is in progress, processor can execute non-memory instructions whenever semantically possible

Question 10: (10 pts)

* Max I/O operations = 8/100 \* 4 \* (10^6) = 320,000 Instructions/Sec
* Max # of words = 32 \* (10^4)/3 = 106,777 Words/Sec

Question 11: (10 pts)

Foreground: 8/100 \* 4 \* (10^6) \* 5 = 1,600,000 Machine cycles

Background: 92/100 \* 4 \* (10^6) \* 2 = 7,360,000 Machine cycles

Total = 8,960,000 Machine cycles = 8,960,000 Words/Sec

Question 12:

* (5 Pts.) 0.99%--Please see HW/class notes for solution
* (5 Pts.) 3960—Please see HW/class notes for solution

Question 13:

* (5 Pts.) Write mechanism--Block read, block erase, block write
* (5 Pts.) Wear leveling algorithm spreads writes across blocks

Question 14:

Bus arbitration using daisy chaining (please see class notes)

* BPRN line travels to BPRO if the module has not raised request
* Bus control granted to the module with BPRN != BPRO
* Address vector identifying device put on separate bus
* Arbitration completed within a clock cycle